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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,576	07/29/2002	Jung-An Wang	9445-US-PA	3242

31561 7590 05/17/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
AMIN, NIRAV S	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,576	WANG ET AL.	
	Examiner	Art Unit	
	Nirav S. Amin	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Tran et al. (USPN: 6,253,319) herein after referred to as Tran.

As per claim 1, Tran discloses:

a datapath chipset, having a peripheral configuration memory for storing an effective peripheral configuration value;

a power-supply/memory-clearing selecting circuit for switching between a power-supply status and a memory-clearing status for the peripheral configuration memory [Figure 4; Column 5, lines 60-64]; and

a latching circuit, electrically coupled to and in between the power-supply/memory-clearing selecting circuit and the datapath chipset for providing a clearing latch signal when the power-supply status is switched to the memory-clearing status [Figure 4; Column 6, lines 27-55].

As per claim 7, Tran discloses:

a power-supply/memory-clearing selecting circuit for switching between a power-supply status and a memory-clearing status [Figure 4; Column 5, lines 60-64]; and

a datapath chipset electrically coupled to the power-supply/memory-clearing selecting circuit, the datapath chipset comprising a peripheral configuration memory for storing an effective peripheral configuration value and a latching circuit for providing a clearing latch signal when the power-supply status is switched to the memory-clearing status [Figure 4; Column 6, lines 27-55].

As per claim 13, Tran discloses:

a power-supply/memory-clearing selecting circuit for switching between a power-supply status and a memory-clearing status for the peripheral configuration memory [Figure 4; Column 5, lines 60-64]; and

a latching circuit, electrically coupled to the power-supply/memory-clearing selecting circuit for providing a clearing latch signal when the power-supply status is switched to the memory-clearing status [Figure 4; Column 6, lines 27-55].

As per claim 17, Tran discloses:

reading the clearing latch signal [Column 6, lines 44-55];

writing a clearing value into the peripheral configuration memory when the clearing latch signal is set [Column 5, lines 25-33]; and

resetting the clearing latch signal [Column 5, lines 32-33; Column 8, line 65-Column 9, line3].

As per claims 2 and 8, Tran discloses:

wherein the datapath chipset is a south bridge (212).

As per claims 4 and 10, Tran discloses:

a basic input/output system (BIOS) that is capable of reading the clearing latch signal via the datapath chipset when the computer switches on, wherein once the clearing latch signal is set, the content of the peripheral configuration memory is cleared and the clearing latch signal is reset [Column 5 lines 32-33].

As per claims 5, 11, 13 and 19, Tran discloses:

wherein the peripheral configuration memory comprises a volatile memory.

As per claims 6, 12, 15 and 20, Tran discloses:

wherein the volatile memory is a complementary metal oxide semiconductor (CMOS) random access memory (RAM).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav S. Amin whose telephone number is (571) 272-3821. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NA

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100